

FIGURE 2

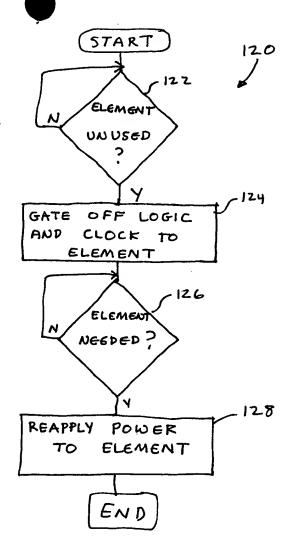


FIGURE 3

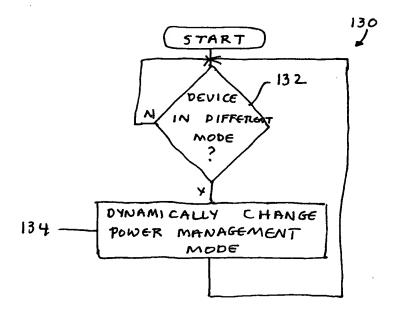


FIGURE 4

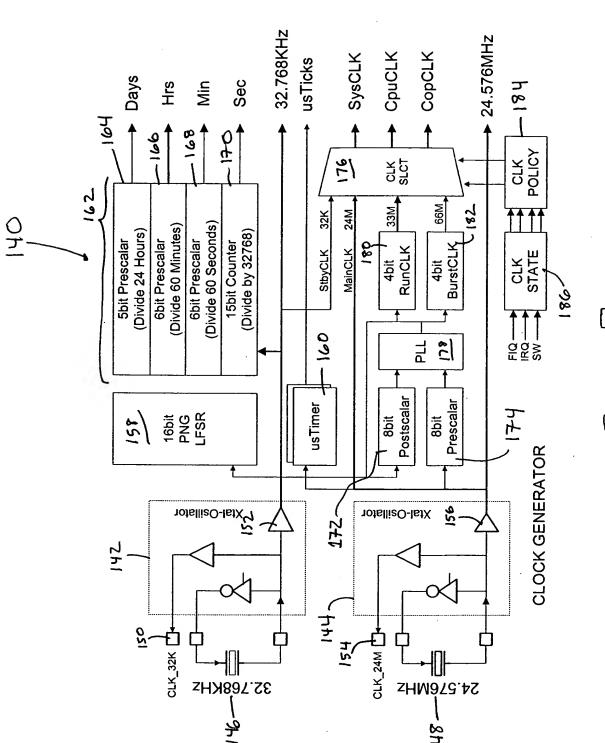


FIGURE 5

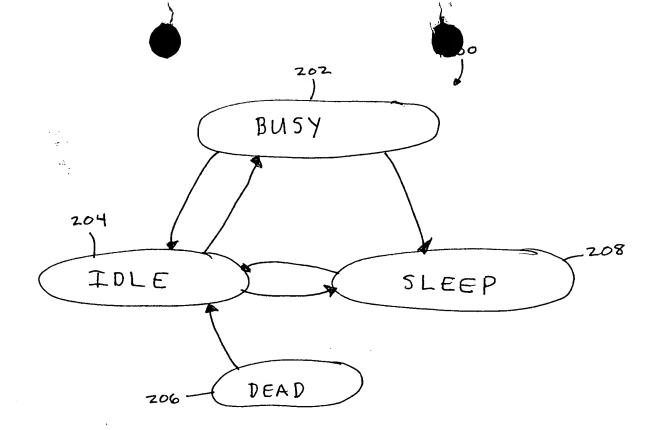


FIGURE 6

220

I. PP6001B POWER MANAGEMENT REGISTER DESCRIPTIONS bit0 bit5 bit4 bit3 bit2 bit1 bit14 bit13 bit12 bit11 bit10 bit9 bit8 bit7 bit6 bit15 AC97 RTC | C.EXT. C.24M C.32K CF00:5000 222 HSTK LCD.C UART .-12C-125 SPDIF THR MHC SMC CFLCD. B CF00:5000 24MHz 32KHz 24MHz 24MHz sysclk sysclk 24MHz 24MHz 24MHz 24MHz 24MHz sysclk 24MHz 32KHz SYSCLK CCH1 * IDE USB GPIO CF00:5004 CCHO rsvd CF00:5004 rsvd sysclk 24/48 sysclk rsvd rsvd rsvd rsvd rsvd rs vd rsvd rsvd rsvd rsvd AUTO rsvd CPU.STATE CF00:5008 AUTO rsvd rsvd rsvd rsvd COF. STATE rsvd CPU. IRQ CPU. MAIN CF00:500C COP.MAIN CPU.FIQ CPU. IDLE COP. IDLE COP.FIQ COP. IRQ CF00:5010 RUN CLK RATE PLL X24N X32K SYS CLK SOURCE BURST CLK RATE rsvd rsvd CF00:5014 rsvd PLL PRESCALAR VALUE CF00:5018 rsvd rsvd rsvd rsvd rsvd rsvd rsvd rsvd 228 PLL POSTSCALAR VALUE CF00:501C rsvd rsvd rsvd rsvd rsvd rsvd rsvd rsvd CF00:5020 FREE RUNNING PLL COUNTER (PNG_LFSR) WDT.E WDT.X W.SYS W.COP W.CPU CF00:502C 0 Z.SWR Z.WDT S.SWR S.WDT P.SWR P.WDT Sys.r cop.r Gyu.r CF00:5030 LED.B LED.E WART SPDIF LGG97 THICK DENE MICH SIE CCH1 CCHO CF00:5034 rsvd rsvd rsvd rsvd rsvd IDE USB GREE rsvd rsvd rsvd

FIGURE 7